

Advanced Time Synchronization for Highest Precision

Extremely Accurate Clock
and Frame Sync

Embedded PWM



Highly Configurable



Block Diagram



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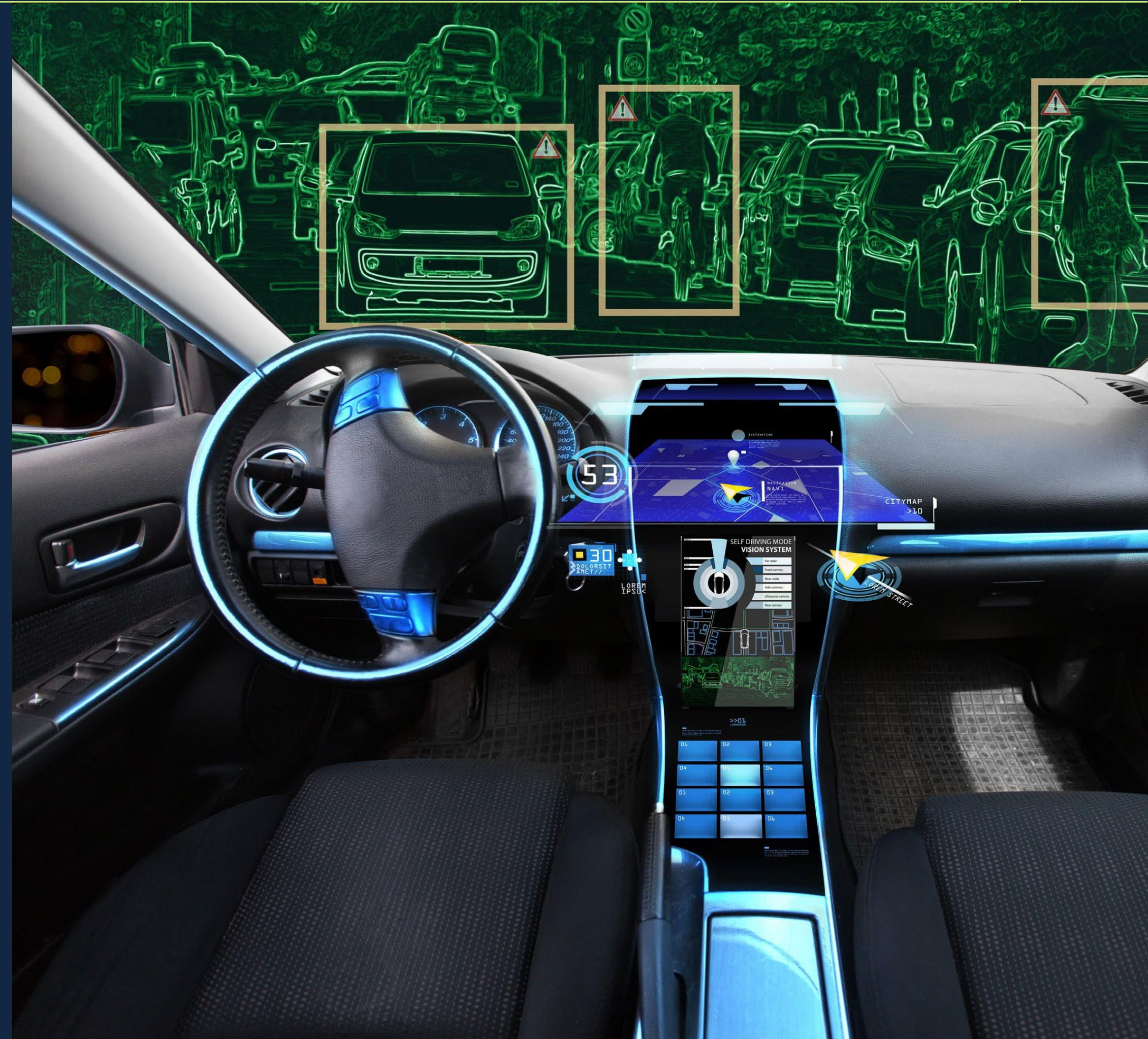
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PWM embedded within the deserializer

- Removes the need for an external PWM circuit, including programmable components such as an FPGA or CPLD, significantly **reducing system cost** and shortening the design cycle.

Best in class: Less than 100 nanoseconds of jitter

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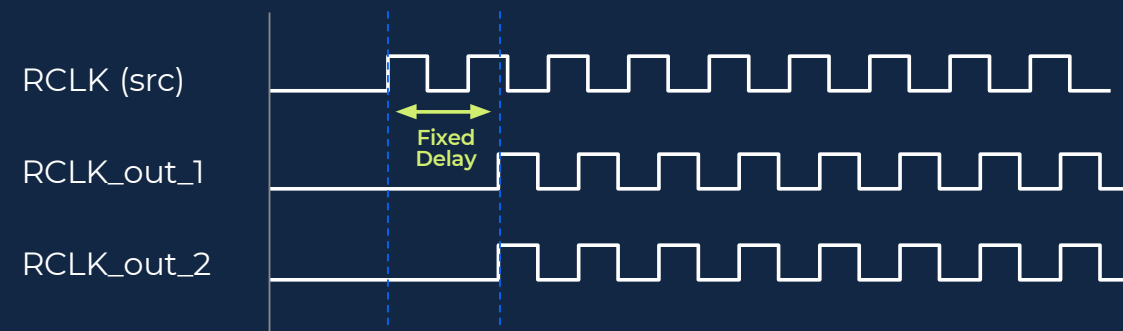
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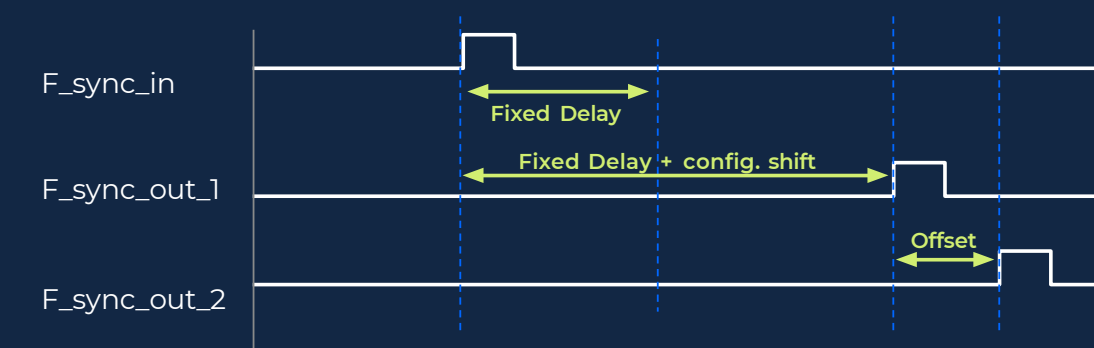
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Highly configurable PWM

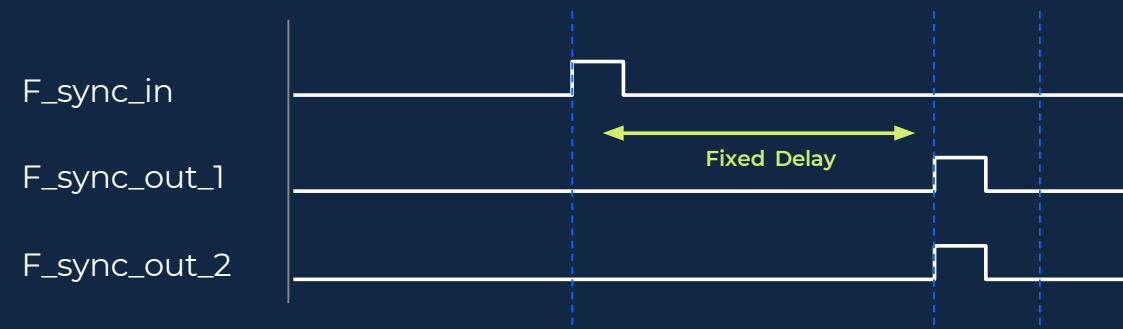
Clock Sync, Fixed Delay



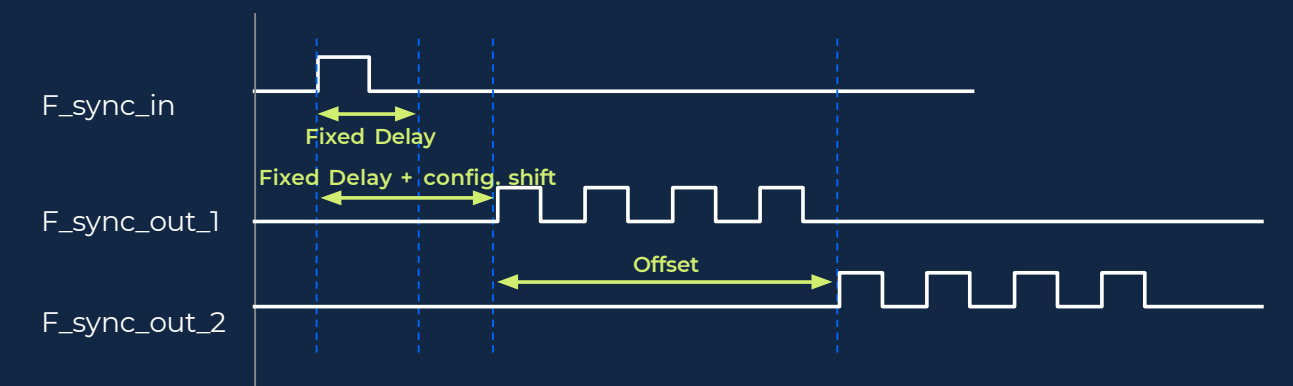
Frame Sync Pulses, Fixed Delay + Configurable Shift + Offset



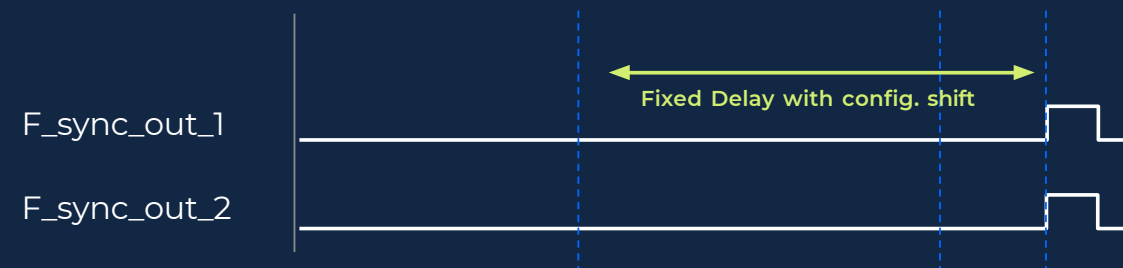
Frame Sync, Fixed Delay



Periodic Synced Pulses + Configurable Shift + Configurable Offset



Frame Sync Pulses, Fixed Delay + Configurable Shift



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